

NOV 20 2006

PTO/SB/17 (07-08)

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Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

## FEE TRANSMITTAL

### For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

<b>TOTAL AMOUNT OF PAYMENT</b>		(\$)		500.00
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**METHOD OF PAYMENT** (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ Note ☐ Other (please identify):

☒ Deposit Account Deposit Account Number: 09-0458 Deposit Account Name: IBM Corporation (Fishkill)

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

### FEE CALCULATION

**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

**2. EXCESS CLAIM FEES**

Fee Description

Each claim over 20 (including Reissues)

Each independent claim over 3 (including Reissues)

Multiple dependent claims

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

**3. APPLICATION SIZE FEE**

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
7	-40 =	x		
HP = highest number of total claims paid for, if greater than 20.				
1	-6 =	x		
HP = highest number of independent claims paid for, if greater than 3.				

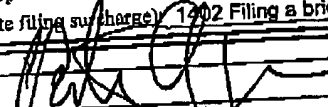
**4. OTHER FEE(S)**

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge), 1202 Filing a brief in support of an appeal

Non-English Specification	\$130	
Other (e.g., late filing surcharge), 1202 Filing a brief in support of an appeal		500.00

**SUBMITTED BY**

Signature: 

Name (Print/Type): Burton A. Amernick

Registration No. (Attorney/Agent): 24,852

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Date: November 20, 2006

NOV 20 2006

**FAX TRANSMISSION**

DATE: November 20, 2006

PTO IDENTIFIER: Application Number 09/611,955-Conf. #6678  
Patent Number

Inventor: Cyprian E. Uzoh et al.

MESSAGE TO: US Patent and Trademark Office

FAX NUMBER: (571) 273-8300

FROM: CONNOLLY BOVE LODGE & HUTZ LLP  
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Attorney Dkt #: 20136-00318-US

PAGES (Including Cover Sheet): 15

CONTENTS: Fee Transmittal (1 page)  
Appeal Brief (12 pages)  
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Certificate of Transmission (1 page)

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U. S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Application No. (if known): 09/611,955

Attorney Docket No.: 20138-00318-US

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Fee Transmittal (1 page)

Appeal Brief (12 pages)

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Docket No.: 20136-00318-US  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:  
Cyprian E. Uzoh et al.

Application No.: 09/611,955

Filed: July 6, 2000

For: METHOD TO SELECTIVELY FILL  
RECESSES WITH CONDUCTIVE METAL

Confirmation No.: 6678

Art Unit: 2811

Examiner: H. K. Vu

**APPEAL BRIEF**

MS Appeal Brief - Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

11/21/2006 HDEHESS1 00000088 090458 09611955  
01 FC:1402 500.00 DA

Dear Sir:

As required under § 41.37(a), this brief is filed more than two months after the Notice of Appeal filed in this case on September 18, 2006, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying  
TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

- |            |                                               |
|------------|-----------------------------------------------|
| I.         | Real Party In Interest                        |
| II.        | Related Appeals and Interferences             |
| III.       | Status of Claims                              |
| IV.        | Status of Amendments                          |
| V.         | Summary of Claimed Subject Matter             |
| VI.        | Grounds of Rejection to be Reviewed on Appeal |
| VII.       | Argument                                      |
| VIII.      | Claims                                        |
| Appendix A | Claims                                        |

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Appendix B Evidence  
Appendix C Related Proceedings

**I. REAL PARTY IN INTEREST**

The real party in interest for this appeal is: International Business Machines Corporation.

**II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS**

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

**III. STATUS OF CLAIMS****A. Total Number of Claims in Application**

There are 32 claims pending in application.

**B. Current Status of Claims**

1. Claims canceled: 1-24
2. Claims withdrawn from consideration but not canceled: 0
3. Claims pending: 25-32
4. Claims allowed: 0
5. Claims rejected: 25-32

**C. Claims On Appeal**

The claims on appeal are claims 25-32

**IV. STATUS OF AMENDMENTS**

Applicant did not file an Amendment After Final Rejection.

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## V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a semiconductor structure. The semiconductor structure of the present invention as recited in independent claim 25 comprises a semiconductor substrate (see page 6, line 13 and page 22, original claim 25 lines 1 and 2), a recess 2 located in at least one major surface of the semiconductor substrate (see page 1, lines 14-16; Figure 1; page 22, original claim 25, lines 2 and 3; and original abstract of disclosure);

an electrical insulating layer 3 located over the at least one major surface and in said recess (page 7, lines 20-23 and Figure 1);

a conductive barrier 4 located over the insulating layer in the recess and over the at least one major surface (page 8, lines 1 and 2 and Figure 1);

a plating seed layer 6 over the conductive barrier within the recess only (page 6, lines 17-19; page 8, lines 18-19; Figure 1; original claim 25, lines 5-7); and  
a conductive metal 8 in the recess only (page 6, lines 19-20; page 10, lines 4-5; Figure 3; page 23, original claim 25, lines 7-8).

According to claim 26, the barrier 4 comprises a layer of tantalum nitride adjacent said insulating layer and a layer of tantalum above said tantalum nitride layer (page 8, lines 1-8).

According to claim 27, the tantalum nitride layer is about 15 to about 500 Å thick and said tantalum layer is about 500 to about 5000 Å thick (page 8, lines 1-11).

According to claim 28, the seed layer 6 is copper (page 8, lines 20-21).

According to claim 29, the copper seed layer 6 is sputtered copper (page 8, lines 20-21).

According to claim 30, the copper seed layer 6 is about 100 to about 2000 Å thick (page 8, lines 26-27).

According to claim 31, the conductive metal 8 is copper (page 10, line 4).

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According to claim 32, the conductive metal 8 is about 4000 Å to about 30,000 Å thick (page 12, lines 7-8).

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

- A. Do Claims 25-32 satisfy the definiteness requirements of 35 U.S.C. § 112, second paragraph in the recitations "a conductive barrier located over said insulation layer in said recess and over said at least one major surface" and "a conductive metal in said recesses only"?
- B. Has the Examiner established that Claims 25 and 28-32 are obvious and therefore unpatentable under 35 USC 103 over the cited art and namely over US Patent 5,821,168 to Jain in view of US Patent 4,577,395 to Shibata?
- C. Has the Examiner established that Claims 26 and 26 are obvious and therefore unpatentable under 35 USC 103 over the cited art and namely over US Patent 5,821,168 to Jain in view of US Patent 4,577,395 to Shibata and further in view of US Patent 6,329,284 to Maekawa?

## VII. ARGUMENT

- A. Claims 25-32 satisfy the requirements of 35 USC 112, second paragraph
- Claims 25-32 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite in the use of the recitations "a conductive barrier located over said insulation layer in said recess and over said at least one major surface" and "a conductive metal in said recesses only". This rejection is not deemed tenable.

The specification expressly discloses providing a conductive barrier located over the insulation layer. For example, page 8, lines 1 and 2 state:

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"Next, a conductive barrier 4 is provided over the insulating layer." Also see Figure 3.

The specification also expressly discloses "a conductive metal in said recesses only."

Along these lines, see page 6, lines 19-22, which states:

"An electroplated conductive metal is located in the recesses only... and not on other portions of the substrate."

Also see page 10, lines 9 and 10, which states:

"The conductive metal does not plate on the barrier layer but instead preferably plates on the seed layer." The seed layer remains in the recesses only (see page 6, lines 18-19).

Accordingly, at this stage, the conductive metal only plates in the recesses, not on the major surface of the substrate, even though small amounts of excess of conductive metal might exist above the recesses. Therefore, as stated at page 12, lines 11-27 of the original disclosure, the conductive material 8 can then be chemically-mechanically polished to remove small amounts of metal above the surface of the recesses. Typical polishing slurries contain colloidal silica. At this point and prior to removal of the barrier layer 5, all of the claimed recitations are disclosed. Claiming a structure at this stage is entirely proper.

It is only, after removal of the small amounts of metal above the surface of the recesses, is the barrier layer 5 removed. For example, see page 12, lines 16 and 17 that state:

"Next, the barrier layer 5 and plated metal is removed down to the insulating layer 3 (see Fig. 4)." (emphasis mine)



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For a similar disclosure, also see figure 7.

- B. Claims 25 and 28-32 are not rendered unpatentable by US Patent 5,821,168 to Jain in view of US Patent 4,577,395 to Shibata.

Claims 25 and 28-32 were rejected under 35 USC 103 as being unpatentable over US Patent 5,821,168 to Jain in view of US Patent 4,577,395 to Shibata. The cited references fail to render obvious claims 25 and 28-32.

As appreciated by the examiner, the recesses 72 in insulating layer 52 of Jain do not exist in a semiconductor substrate as recited in the claims. The recesses exist only on the substrate. In fact, the recesses (i.e. interconnect channels) in Jain referred to in the office action cannot exist in the semiconductor substrate since they must be present above the interconnects 28. Therefore, in view of the process and structure required by Jain, the recesses cannot exist in the semiconductor substrate. To include the recesses in the semiconductor substrate would be contrary to the objectives of Jain and defeat the purposes of the reference.

US Patent 4,577,395 to Shibata fails to overcome the above discussed deficiencies of Jain with respect to rendering unpatentable the above claims since, among other things, Shibata is not even properly combinable with Jain. As stated above, including the recesses in the semiconductor substrate would be contrary to the objectives of Jain and defeat the purposes of Jain. Where the proposed modification would be contrary to the objectives of the cited reference, the rejection is not proper. For example, see *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984). Moreover, Shibata does not include a barrier layer or metal in the recesses.

- C. Claims 26 and 27 are not rendered unpatentable by US Patent 5,821,168 to Jain in view of US Patent 4,577,395 to Shibata and further in view of US Patent 6,329,284 to Maekawa.

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Claims 26 and 27 were rejected under 35 USC 103 as being unpatentable over US Patent 5,821,168 in view of US Patent 4,577,395 to Shibata and further in view of US Patent 6,329,284 to Maekawa. The cited references fail to render obvious claims 26 and 27. US Patent 6,329,284 to Maekawa fails to overcome the above discussed deficiencies of Jain and Shibata with respect to rendering unpatentable the present claims. In addition, the presence of a layer of tantalum nitride and a layer of tantalum as recited in claims 27 and 27 would not be present in Jain because of the process required by Jain which involves nitriding of the oxide dielectric. See column 2, lines 35-38. To include layers of tantalum nitride and a layer of tantalum as mentioned by Maekawa would be contrary to the stated objections of Jain and therefore not an obvious modification. As mentioned above, where the proposed modification would be contrary to the objectives of the cited reference, the rejection is not proper. For example, see *In re Gordon, supra*.

#### Discussion of Case Law of Interest

The mere fact that cited art may be modified in the manner suggested in the Office Action does not make this modification obvious, unless the cited art suggest the desirability of the modification. No such suggestion appears in the cited art in this matter. The Board's attention is kindly directed to *In re Lee* 61 USPQ2d 1430 (Fed. Cir. 2002) *In re Dembiczak et al.* 50 USPQ2d. 1614 (Fed. Cir. 1999), *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984), *In re Laskowski*, 10 USPQ2d. 1397 (Fed. Cir. 1989) and *In re Fritch*, 23, USPQ2d. 1780 (Fed. Cir. 1992).

In *Dembiczak et al.*, *supra*, the Court at 1617 stated: "Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. See, e.g., C.R. Bard, Inc., v. M3 Sys., Inc., 157 F.3d. 1340, 1352, 48 USPQ2d. 1225, 1232 (Fed. Cir. 1998) (describing 'teaching or suggestion motivation [to combine]' as in 'essential evidentiary component of an obviousness holding'), *In re Rouffet*, 149 F.3d 1350, 1359, 47 USPQ2d. 1453, 1459 (Fed. Cir. 1998) ('the Board must identify specifically...the reasons one of ordinary skill in the art would have been motivated to select the references and combine them');...".

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The present invention could only be derived from the cited art by the use of "hindsight", i.e. by knowing what Applicants' invention was in advance from Applicants' disclosure, and then *ex post facto* reconstructing Applicants' invention from the prior art after a thorough search. It is impermissible under 35 U.S.C. 103 to use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. See *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Furthermore, it is well settled that hindsight reconstruction using the patent application as a guide through the maze of prior art references, combining "the right references in the right way" so as to achieve the result of the claimed invention must be avoided. See *Grain Processing Corp. v. American Maize-Products Corp.*, 5 U.S.P.Q.2d 1788 (Fed. Cir. 1988).

#### VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Applicant on October 19, 2001.

Dated: November 20, 2006

Respectfully submitted,

By   
Burton A. Amernick

Registration No.: 24,852  
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Attorney for Applicant

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**RECEIVED  
CENTRAL FAX CENTER****NOV 20 2006****APPENDIX A****Claims Involved in the Appeal of Application Serial No. 09/611,955**

25. A semiconductor structure, comprising: a semiconductor substrate; a recess located in at least one major surface of said semiconductor substrate; an electrical insulating layer located over said at least one major surface and in said recess; a conductive barrier located over said insulating layer in said recess and over said at least one major surface; a plating seed layer located over said conductive barrier within said recess only; and a conductive metal in said recess only.

26. The semiconductor structure of claim 25 wherein said barrier comprises a layer of tantalum nitride adjacent said insulating layer and a layer of tantalum above said tantalum nitride layer.

27. The semiconductor structure of claim 26 wherein said tantalum nitride layer is about 15 to about 500 Å thick and said tantalum layer is about 500 to about 5000 Å thick.

28. The semiconductor structure of claim 25 wherein said seed layer is copper.

29. The semiconductor structure of claim 28 wherein said copper is sputtered copper.

30. The semiconductor structure of claim 28 wherein said copper is about 100 to about 2000 Å thick.

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31. The semiconductor structure of claim 25 wherein said conductive metal is copper.
32. The semiconductor structure of claim 31 wherein said conductive metal is about 4000 Å to about 30,000 Å thick.

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APPENDIX B

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No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

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Docket No.: 20136-00318-IJS

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APPENDIX C

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.